Signaling Concerns in Intra-cabinet 4.25 Gbit/s

Equalization

- Three predominant compensation techniques are used at present signaling rates.
  - Pre-emphasis
    - Occurs at transmitter
    - High frequency component of launch amplitude is increased ('peaked') to compensate for higher loss of high frequency components as they propagate through lossy transmission media such as FR4 (or low frequency component is decreased; effect is the same)
    - The effects of pre-emphasis on waveform are observable in the transmission media.

- Post equalization
  - Occurs in the receiver
  - May or may not be adaptive
  - Active or passive circuitry in the receiver selectively amplifies (or limits) the different frequency components of the incoming signal. Different frequency components are amplified (or limited) differently from other frequency components to compensate for the frequency dependent attenuation of lossy transmission media such as FR4.
  - Equalizer's effect on the signal is not observable.

- Passive or active equalization in the transmission path
  - Occurs in transmission media.
  - Either passive or active components are added to a transmission structure (such as a cable assembly) to compensate for the frequency dependent attenuation of the structure's transmission media.
  - The effects of the manipulation of the waveform are observable in the transmission media.

•Which of these signal conditioning techniques should be promoted/allowed in 4.25Gbit/s FC variant?

- •Transmitter pre-emphasis
  - •Receiver post equalization
    - •Equalization in the transmission path

•A compliance channel was used in the Xaui specification as a method of allowing transmitter pre-emphasis.

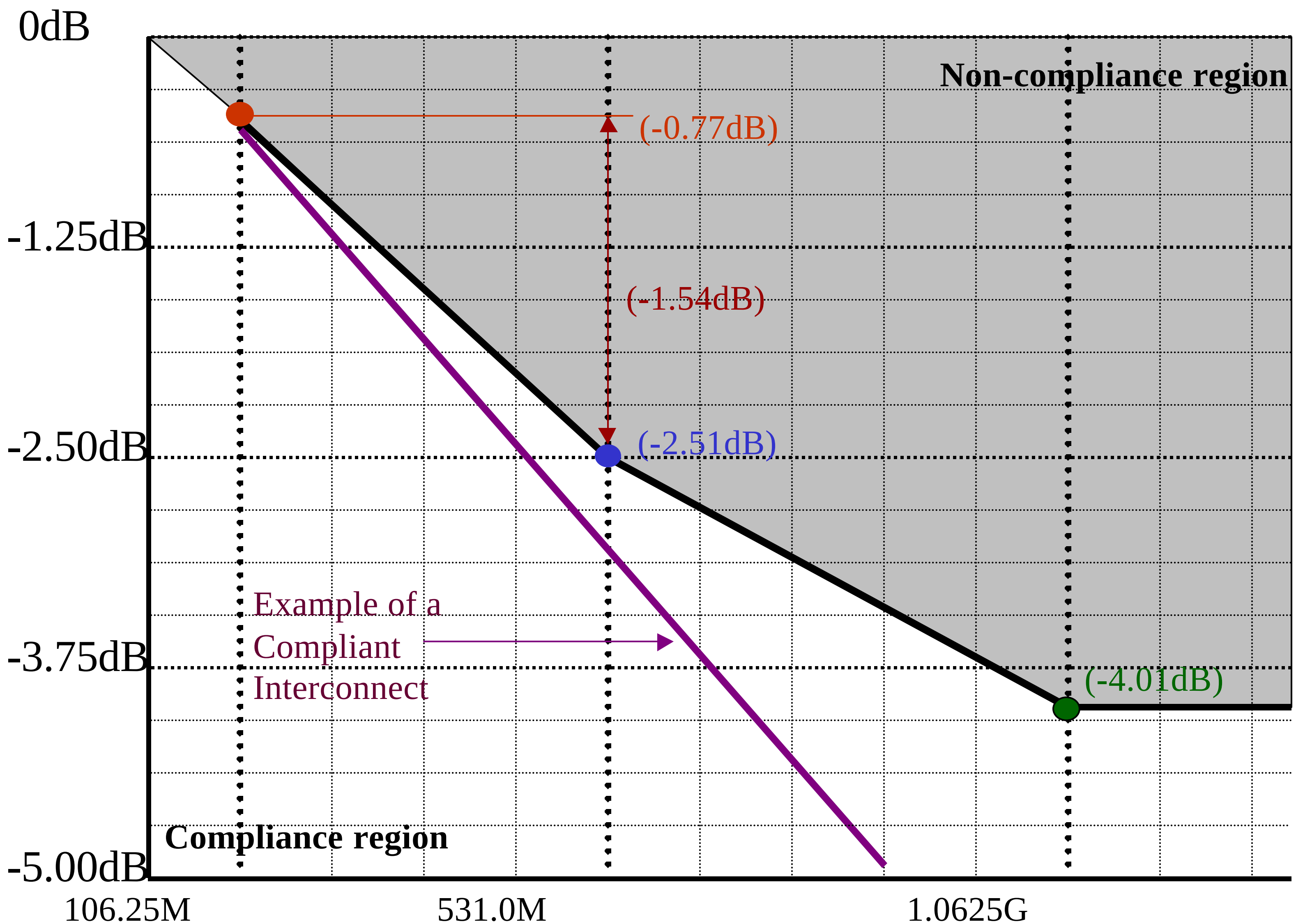
•The formula from Xaui is mathematically representative of ~50cm of FR4 PCB trace.

$S_{21} = -\ 20*(\log_{10}\mathbf{e}^{1})*[a_1*\mathrm{sqrt}(f) + a_2*(f) + a_3*(f)^2\ ]$ Db
where $a_1 = 6.5e\text{-}6$, $a_2 = 2.0e\text{-}10$, $a_3 = 3.3e\text{-}20$

If the equation from Xaui had been applied to 1Gbit/s FC, the defining points would have occurred at 106.25Mhz, 531Mhz, and 1062.5Mhz. Minimum allowed ISI is defined at the lowest and highest bit rate frequencies. The maximum attenuation is defined at 10x the lowest frequency.

	Constants from Xaui			
	a1 =	6.50E-06		
	a2 =	2.00E-10		
	a3 =	3.30E-20		
1.0625 Gbit/s FC				
106,250,000	-8.686	**-0.77**		
212,500,000	-8.686	**-1.21**		
318,750,000	-8.686	**-1.59**		
425,000,000	-8.686	**-1.95**		
531,250,000	-8.686	**-2.31**	**-1.54**	<=ISI
637,500,000	-8.686	**-2.65**		
743,750,000	-8.686	**-2.99**		
850,000,000	-8.686	**-3.33**		
956,250,000	-8.686	**-3.67**		
1,062,500,000	-8.686	**-4.01**		

The resulting graph is on the next page.

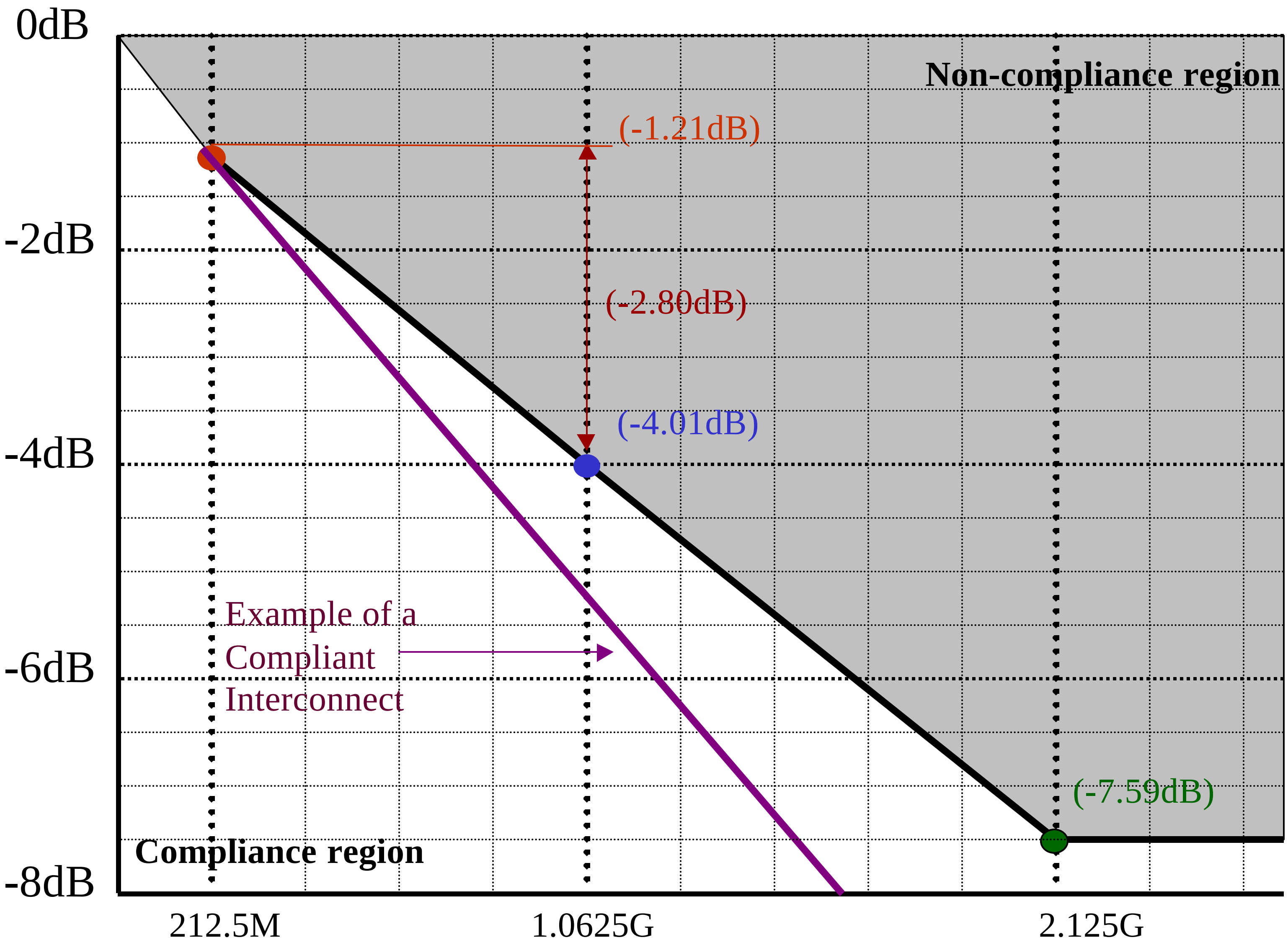


If we would have used the Compliance Interconnect methodology for 1.0625 Gbit/s FC the graph would have looked like this using the Xaui equation

If the equation from Xaui had been applied to 2.125Gbit/s FC, the defining points would have occurred at 212.5Mhz, 1.0625Ghz, and 2.125Ghz.

	a1 =	6.50E-06		
	a2 =	2.00E-10		
	a3 =	3.30E-20		
2.125Gbit/s FC				
212,500,000	-8.686	**-1.21**		
425,000,000	-8.686	**-1.95**		
637,500,000	-8.686	**-2.65**		
850,000,000	-8.686	**-3.33**		
1,062,500,000	-8.686	**-4.01**	**-2.80**	<=ISI
1,275,000,000	-8.686	**-4.70**		
1,487,500,000	-8.686	**-5.40**		
1,700,000,000	-8.686	**-6.11**		
1,912,500,000	-8.686	**-6.84**		
2,125,000,000	-8.686	**-7.59**		

The resulting graph is on the next page.

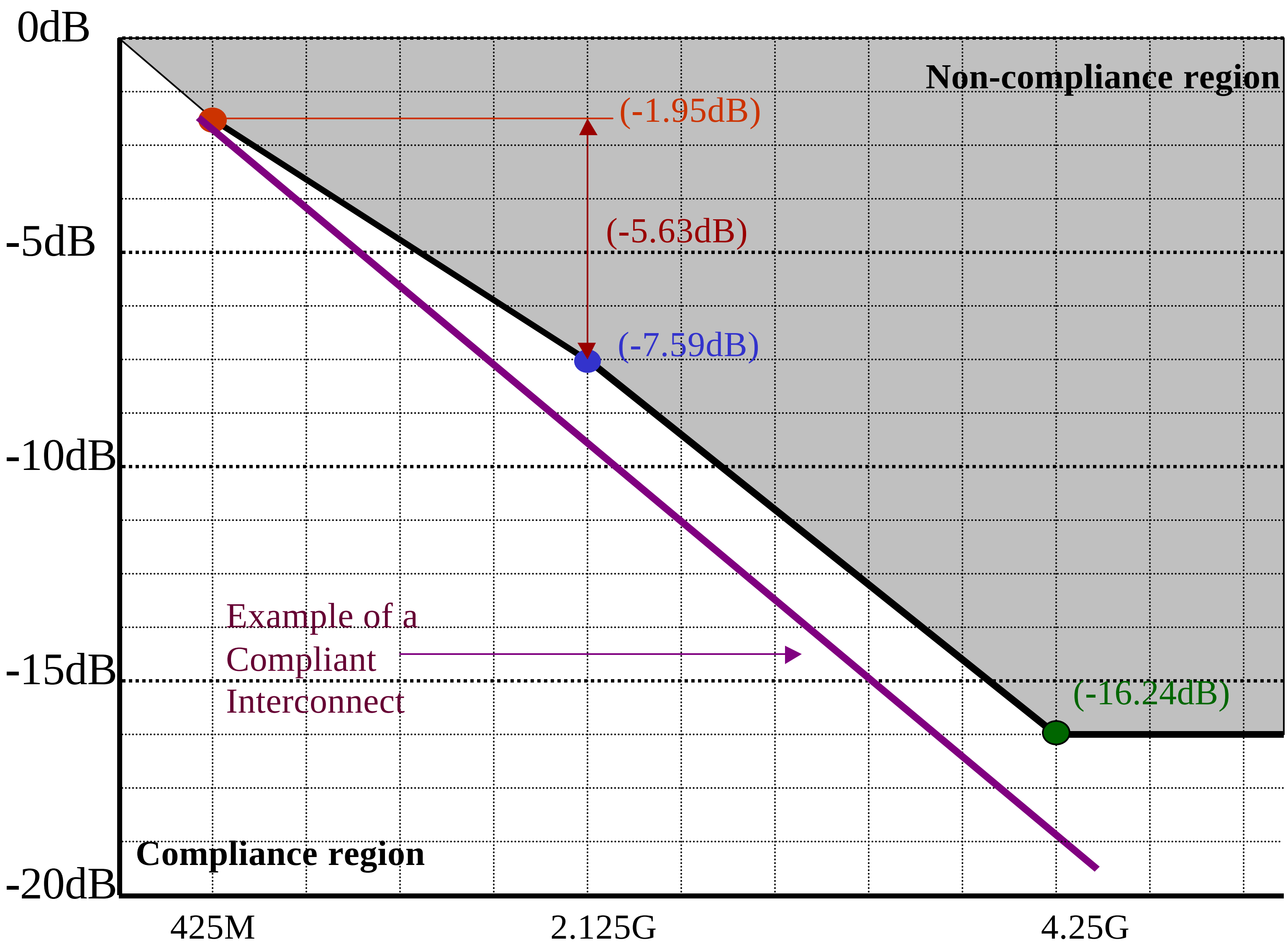


If we would have used the Compliance Interconnect methodology for 2.125 Gbit/s FC the graph would have looked like this.

Appling the equation from Xaui to 4.25Gbit/s FC, the defining points will occur at 425Mhz, 2.125Ghz, and 4.25Ghz.

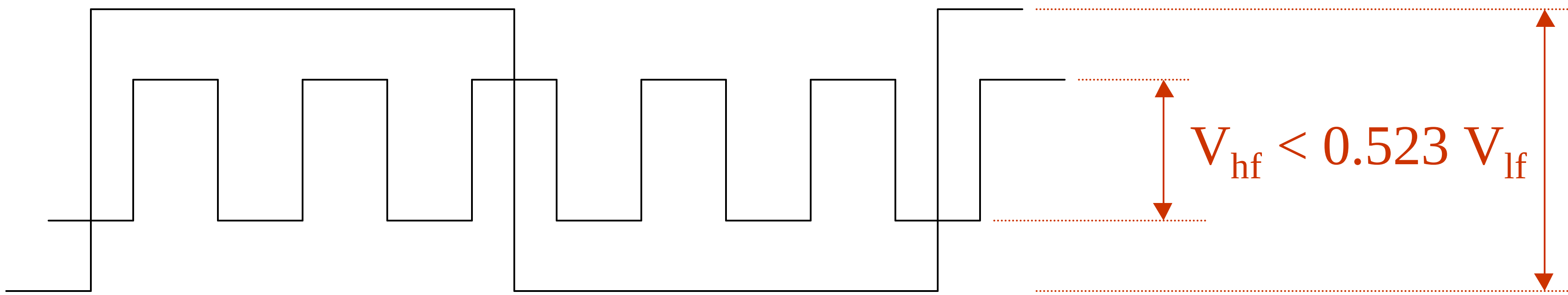
	a1 =	6.50E-06		
	a2 =	2.00E-10		
	a3 =	3.30E-20		
4.250 Gbit/s FC				
425,000,000	-8.686	**-1.95**		
850,000,000	-8.686	**-3.33**		
1,275,000,000	-8.686	**-4.70**		
1,700,000,000	-8.686	**-6.11**		
2,125,000,000	-8.686	**-7.59**	**-5.63**	<=ISI
2,550,000,000	-8.686	**-9.14**		
2,975,000,000	-8.686	**-10.78**		
3,400,000,000	-8.686	**-12.51**		
3,825,000,000	-8.686	**-14.33**		
4,250,000,000	-8.686	**-16.24**		

The resulting graph is on the next page.



COMPLIANCE INTERCONNECT GRAPH FOR 4.25 Gbit/s FC

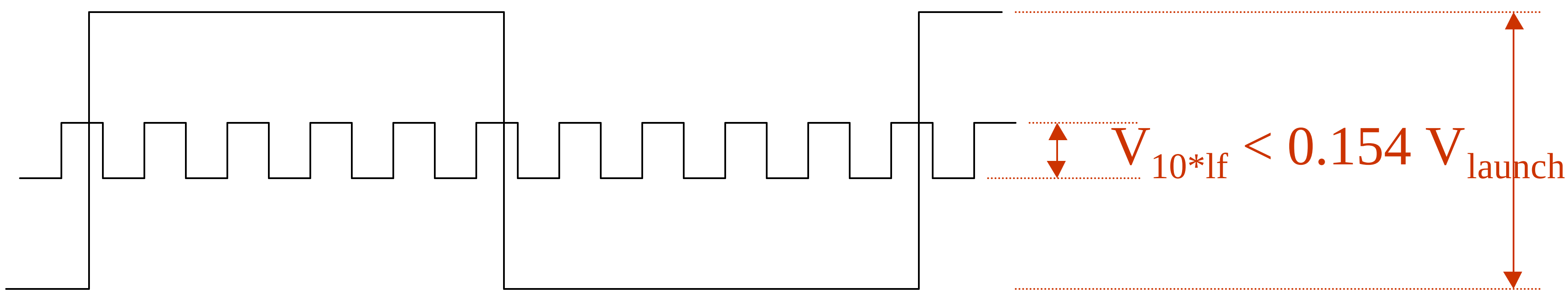
There are two defining criteria for the minimum 4.25Gbit/s FC Compliance Interconnect. First, the ISI attenuation number (-5.63dB) must be exceeded. The amplitude of the high frequency component of the encoded waveform (2.125Ghz) must be less than 0.523 times the amplitude of the lowest frequency component of the encoded waveform (425Mhz) for the channel to be compliant.



Note: $V_{lf} = 0.799\ V_{launch}$ (-1.95dB)

$V_{hf} = 0.417\ V_{launch}$ (-7.59dB)

Second, the amplitude of a signal ten times the lowest encoded frequency must have an amplitude less than 0.154 times the amplitude of the lowest frequency component of the encoded waveform (-16.24dB)



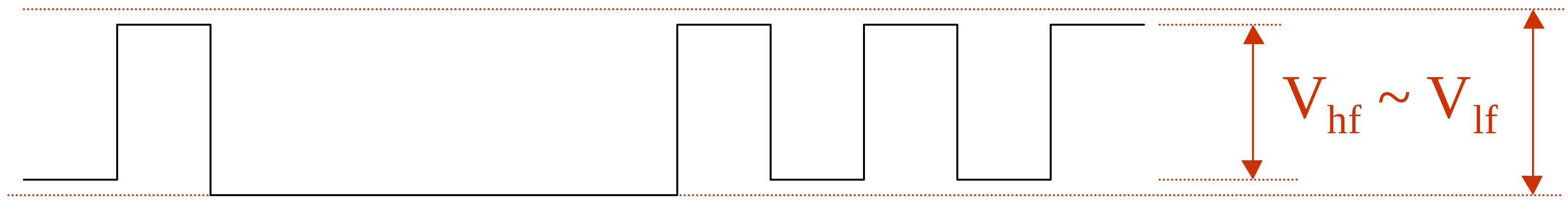
These signal amplitudes are measured at the end of the Compliance Interconnect. Launch amplitudes into the Compliance interconnect must be equivalent without any signal conditioning present when verifying these losses.

An alternate method would be to measure the S21 parameters of the Compliance Interconnect and insure that it's attenuation is greater than the attenuation of the mathematical limits imposed by the Compliance Interconnect equation.

So, why a compliance interconnect?

To allow techniques such as pre-emphasis (or de-emphasis) to compensate for the frequency dependent losses of the Compliance Interconnect.

With Pre-emphasis, high frequency amplitudes are launched into the Compliance Interconnect at a higher amplitudes than the low frequency component, resulting in the amplitudes being similar at the end of the interconnect (if launch difference is ~equivalent to the ISI attenuation delta).



But, there at least three types of equalization (possibly more): transmitter pre-emphasis; receiver post equalization; or equalization in the transmission path.

Should transmitter pre-emphasis be expected to compensate for the entire –5.63dB of ISI attenuation delta permissible by the compliance interconnect At 4.25Gbit/s (this would obviate the need for receiver equalization) {the Xaui model?}?

Or, should the receiver equalization be required to compensate for the entire –5.63dB of permissible ISI attenuation delta (no pre-emphasis be allowed) {the SCSI model?}?

Or should the compensation budget be divided: the transmitter would be required to compensate for ~3.0dB of ISI attenuation delta, while the receiver would be required to tolerate/compensate for the other ~3.0db of ISI attenuation delta.

Or, should

the transmitter pre-emphasis be nominally required to compensate for ~2.0dB of the ISI attenuation delta permissible by the compliance interconnect;

the receiver be nominally required to tolerate / compensate for ~2.0dB of the ISI attenuation delta permissible by the compliance interconnect;

and the designers of the paths between transmitters and receivers would be responsible to ensure that paths that deviate from ~4dB of ISI attenuation delta {for instance: < -3dB, or > -5dB) still operate?

Essentially dividing the equalization amongst various sections of the transmission path.

I have no strong preference for the final equalization technique that will be advanced by the ANSI working groups, but a cohesive equalization structure must be promoted.

Inter-operability between devices designed by different vendors will require clearly defined targets.

How do we proceed?
Start by changing to the Compliance Channel methodology to allow techniques such as pre-emphasis to meet receiver jitter specifications at a certain ISI limit.

Is this enough, or do we need to budget equalization: assigning separate budgets for the transmitter, receiver, and transmission path?

Signaling Concerns in Intra-cabinet 4.25 Gbit/s

Intra-Enclosure Impedance @ 4.25Gbit/s

•Clearly, for many reasons, a uniform impedance at 4.25Gbit/s would be advisable (drives at same impedance as backpanel).

•I propose that the impedance for all 4.25Gbit/s FC intra-enclosure copper variants be changed to 100 ohms differential (from the present 150 ohms differential).

•This was proposed at 2.125Gbit/s, and it was defeated.

•Rather than attack this problem with technical arguments (as was done at 2.125Gbit/s), I would like to propose several straw polls as a first step in this debate:

- How many members know of a 2Gbit/s enclosure that was designed with a PCB characteristic impedance of 100 ohms?

  Number =

- How many members know of a 2Gbit/s enclosure that was designed with a PCB characteristic impedance of 150 ohms?

  Number =

- How many members think that 4Gbit/s enclosures will be designed with a PCB characteristic impedance of 100 ohms?

  Number =

- How many members think that 4Gbit/s enclosures will be designed with a PCB characteristic impedance of 150 ohms?

  Number =

Until this point, the ANSI specification for drives has been firmly entrenched at 150 ohms differential.

What is the next logical step?

Signaling Concerns in Intra-cabinet 4.25 Gbit/s

Aligning with other standards to achieve commonality in physical layers devices, such as transceivers

- Some of the parameters in the intra-enclosure table should be modified to align with the values in other standards.

- Xaui and SAS specification for voltage levels at 3.1875 and 3.0 Gbit/s signaling rates should be considered when finalizing 4.25Gbit/s intra-enclosure compliance points.

- Asic vendors who participated in developing these standards evidently acknowledged that their receiver sensitivity has improved, as both Xaui and SAS specify minimum receive eye openings of less than $400mV_{PP}$.

•I would propose a change to 300mV_{PP} (a reduction from the 400mV_{PP} presently specified). However, I would oppose making this change without the consensus agreement of the providers of FC transceivers. Maximum receive amplitude must stay at 2000mV_{PP} to accommodate legacy systems.

•Additionally, due to the increased attenuation that will be encountered at 4.25Gbit/s, I would further propose that the minimum launch amplitude be increased from 600mV_{PP} to at least 1000mV_{PP} (Note: 1000 * 0.417 (-7.59dB) = 417mV

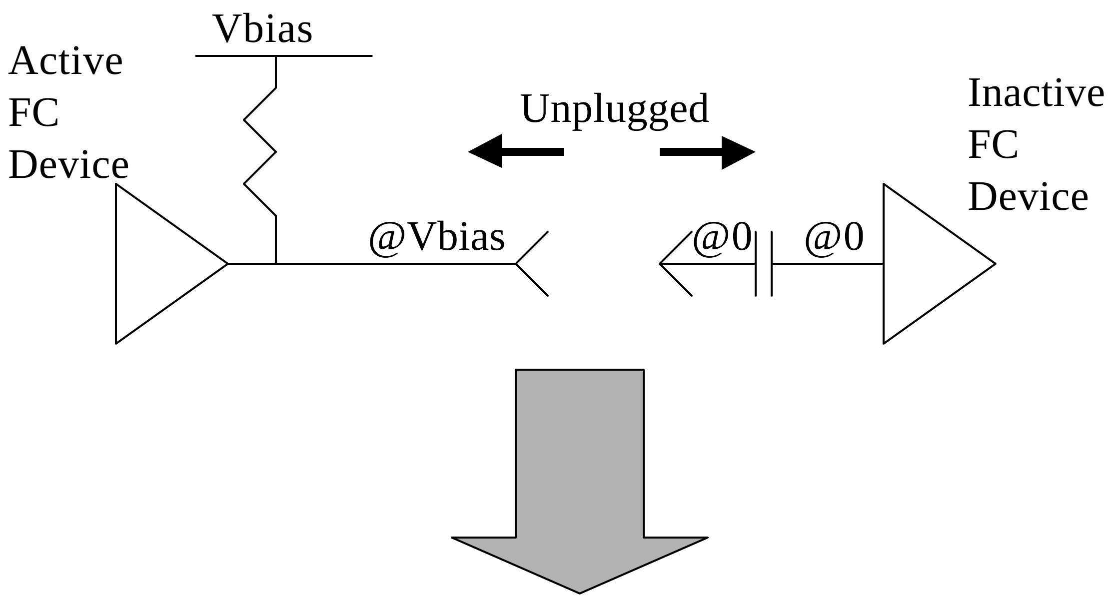
• I propose that the Chair of the Copper Working group set aside time at upcoming meetings for active discussion of these changes.

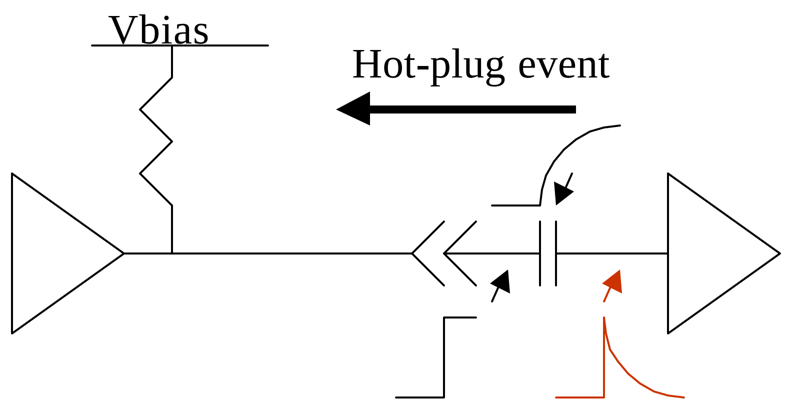
Asic vendors shall be informed (by whatever inclusive method is determined by the working group) so that they have ample time to evaluate the proposed change from 400mV to 300mV at Br, and of the proposed change to a minimum launch amplitude of 1000mV at Bt, at 4.25Gbit/s. It should be made clear that if a vendor does not object by either (a) actively presenting at the next meeting or by (b) submitting a written objection to the change to the chair of the Copper Working group (Ed Grivna) or the reflector, then the presumption of those attending the next meeting will be that the change to 300mV at Br, and the change to an increased launch amplitude of 1000mV at Bt, is acceptable.

(Note: it would be reasonable to expect these new limits to also extend to non-specified devices, such as port bypass chips, that are connected to Beta points, and eventually to other specified points, such as Gamma and Delta).

Signaling Concerns in Intra-cabinet 4.25 Gbit/s

Hot Plug Transients





A hot plug event could result in a voltage being generated to the plugged device that exceeds the breakdown voltage of the gates on the plugged devices (especially as operating voltages of future FC receiver devices are lowered).

•The above scenario is being actively addressed by at least two other Standards groups.   Since ‘hot plugging’ is allowed in Fibre Channel, and the ‘hot plug’ voltage range in FC is larger (FC has 5 Volt legacy port bypass devices) than in other newer Standards, this issue certainly needs to be reviewed for FC.

•I therefore propose that this issue be added as an active item to the agenda of the T11.2 Copper Working Group until that group identifies a course of action to avoid any potential problems in FC systems as a result of allowable ‘hot plug’ events (including legacy systems).

•Since this is primarily an ASIC issue, I would assume that the primary responsibility for resolving this issue should fall to the designers of future low voltage FC SERDES devices.