

FIP Clear Virtual Link Reason Codes

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T11/11-064v0

Problem



- When a FIP Clear Virtual Link (CVL) is received by an ENode, there is no mechanism to directly determine why the CVL was transmitted.
- This causes a problem during trace analysis

CVL (Timeout)



- Case 1 - A timeout due to missing VN_Port FIP Keep Alive frames
 - $2.5 * FKA_VN_PERIOD = 225$ seconds by default
- Case 2 - A timeout due to missing ENode FIP Keep Alive frames
 - $2.5 * FKA_ADV_PERIOD = 20$ seconds by default
- In the case of the missing VN_Port FIP Keep Alive frames
 - it is usually impossible to go backward in the trace 225 seconds when any kind of I/O is running since the buffer will wrap
 - As a result it is usually impossible to determine if this is the reason for the CVL
 - One could infer the reason for the CVL based on its contents, but this could potentially require knowledge additional knowledge about the environment that would also not be present in the trace

CVL (VF_Port offline)



- Case 1 - A configuration change is made by the Administrator
 - The user disables the VF_Port
- Case 2 - The fabric is no longer operational
 - The FCF is in AG/NPV mode and all links to the core switch are removed.

Proposed solution



- Create a set of CVL Reason Codes and Reason Code explanations
- Reason Codes
 - Timeout
 - VF_Port
- Reason Code Explanations
 - VN_Port FIP Keep Alive
 - ENode FIP Keep Alive
 - Configuration Change
 - Fabric Offline

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