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# **Fibre Channel - 10-bit Interface**

Secretariat

**Information Technology Industry Council**

Approved \_\_\_\_\_, 199

**X3 Technical Committee of American National Standards Institute**

## **Abstract**

This Fibre Channel - 10-bit Interface document defines the electrical characteristics of the interface between the physical (FC-0) layer and the transmission protocol (FC-1) layer at the 1 062,5 Mbaud rate. This method of implementation deviates from the method described in FC-PH and allows for lower cost Arbitrated Loop (FC-AL) applications using this specification to interoperate.

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**Foreword** (This Foreword is not part of X3 Technical Report X3.18-199x)

The Fibre Channel - 10-bit Interface defines the electrical characteristics of the interface between the physical (FC-0) layer and the transmission protocol (FC-1) layer at the 1 062,5 MBaud rate. This method of implementation deviates from the method described in FC-PH and allows for lower cost Arbitrated Loop (FC-AL) applications using this specification to interoperate.

This technical report was developed by Task Group X3T11 of Accredited Standards Committee X3 starting in 1994. The technical report approval process started in 1995. This document includes one annex which is informative and is not considered part of the technical report.

Request for interpretation, suggestions for improvement or addenda, or defect reports are welcome. They should be sent to the X3 Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

This technical report was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Technology, X3. Committee approval of the technical report does not necessarily imply that all committee members voted for approval. At the time it approved this technical report, the X3 Committee had the following members:

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## 1 Scope

This document specifies a 10-bit Interface between FC-1 (Transmission protocol layer) and FC-0 (Physical layer) devices at the 1 062,5 MBaud data rate. The document defines the signals, functions and levels of the interface, thus allowing a low cost interface for target applications where cost, size and power determine product success.

In order to insure interoperability between vendors of Physical and Protocol devices the document describes two interfaces between the Physical and Transmission protocol layer. The two interfaces are: Transmit Interface and Receive Interface. Figure 1 shows the relationship of these interfaces between the Physical and Transmission protocol layer.

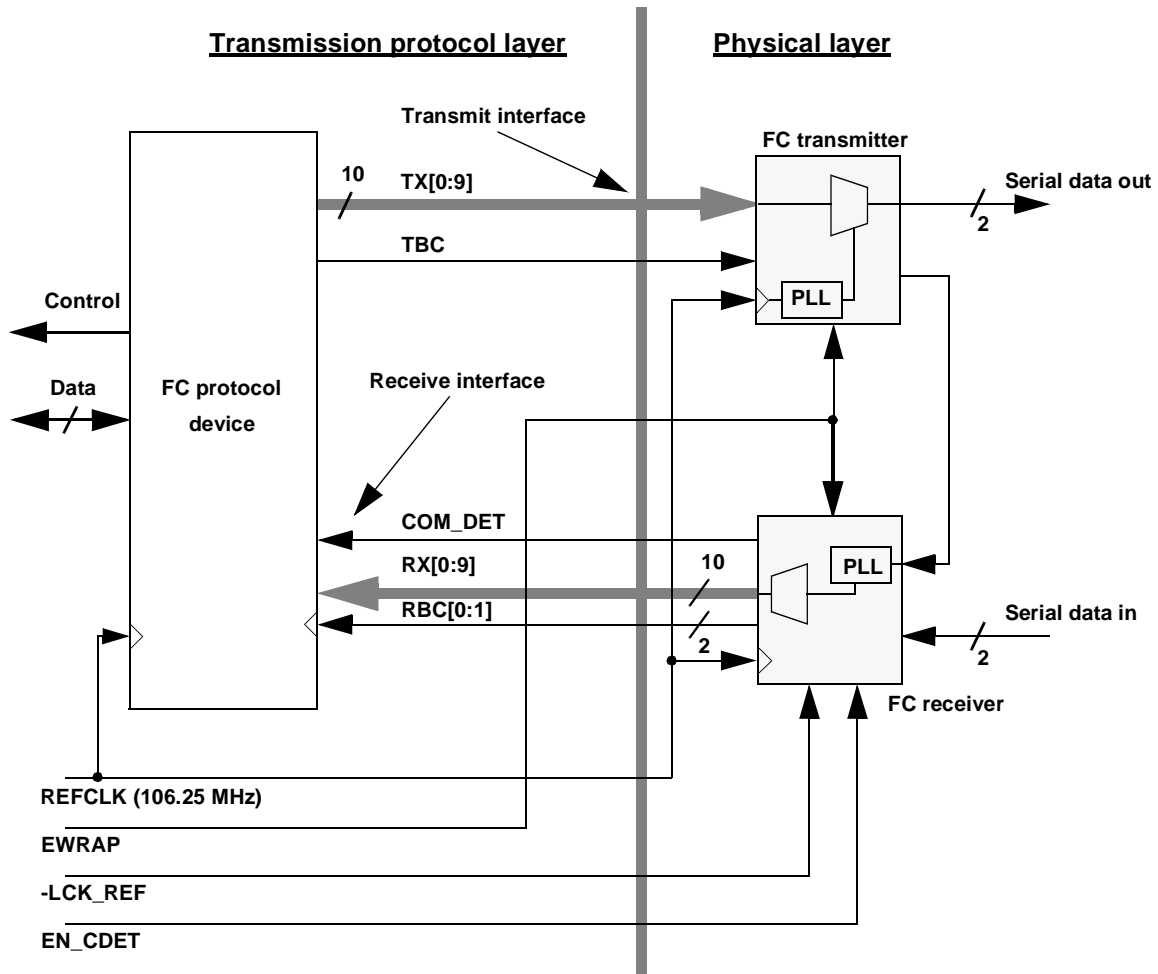


Figure 1 - 10-bit interface diagram

## 2 Normative references

The following American National Standards contain provisions which, through reference in ANSI X3.230, FC-PH, constitute provisions of this Technical Report. At the time of publication, the editions indicated were valid. All standards are subject to revisions, and parties to agreements based on this Technical Report are encouraged to investigate the

possibility of applying the most recent editions of the standards. Members of IEC and ISO maintain registers of currently valid International Standards. ANSI performs a similar function for American National Standards.

ANSI X3.230-1995, *Fibre Channel Physical and Signaling Interface (FC-PH)*.

### 3 Definitions and convention

For this Technical Report, the following definitions, conventions, abbreviations, acronyms, and symbols apply in addition to those in FC-PH.

#### 3.1 Definitions

**3.1.1 byte alignment:** The receiver action that resets the existing byte boundary to that of the comma or K28.5 character currently being received.

**3.1.2 byte slipping:** The receiver action that eliminates the 180° phase error between the output data and output byte clock.

**3.1.3 comma+:** The seven bit sequence (0011111) of an encoded data stream.

**3.1.4 comma-:** The seven bit sequence (1100000) of an encoded data stream.

**3.1.5 sliver:** A pulse with a duration which is less than that specified for that signal (e.g., truncated clock signal).

**3.1.6 word alignment:** The process by which an entity determines the location of the four byte boundary (i.e., word) in a continuous byte stream.

#### 3.2 Editorial conventions

In this Technical Report, a number of conditions, mechanisms, sequences, parameters, events states, or similar terms are printed with the first letter of each word in uppercase and the rest in lowercase (e.g., Physical, comma). Any lowercase uses of these words have the normal technical English meaning.

Number items in this Technical Report do not represent any priority. Any priority is explicitly indicated.

The ISO convention of numbering is used; i.e., the thousands and higher multiples are separated by a space and a comma is used as the decimal point. A comparison of the American and ISO conventions are shown:

ISO	American
0,6	0.6
1 000	1,000
1 323 462,9	1,323,462.9

In case of conflict between figure, table, and text, the text shall take precedence. Exceptions to this convention are indicated in the appropriate sections.

In all the figure, tables, and text of this document, the most significant bit of a binary quantity is shown on the left side. Exceptions to this convention are indicated in the appropriate sections.

The term "shall" is used to indicate a mandatory rule. If the mandatory rule is not followed, the results are unpredictable unless indicated otherwise.

If a field or control bit in a frame is specified as not meaningful, the entity which receives the frame shall not check that field or control bit.

#### Hexadecimal notation

Hexadecimal notation is used to represent fields. For example, a three byte D\_ID field containing a binary value of 11111111 11111111 11111010 is denoted by FF FF FA.

#### 3.3 Abbreviations, acronyms and symbols

Abbreviations and acronyms applicable to this Technical Report are listed. Definitions of several of these items are included in clause 3.1 "Definitions".

FC	Fibre Channel
PLL	Phase Lock Loop
ppm	parts per million

## 4 Functional description

This document defines a 10-bit interface between the Transmission protocol layer and the Physical layer in Fiber Channel implementations. The interface is divided into the "Transmit Interface" and the "Receive Interface".

The Transmit Interface is defined as an input to the Physical layer with a 10-bit wide transmit data bus and its associated transmit byte clock. The reference clock is a 106,25 MHz ( $\pm 100$  ppm) signal. The Transmission protocol layer presents data to the Physical layer relative to the rising edge of the transmit byte clock, the Physical layer accepts data on the rising edge of every clock cycle.

The Receive Interface is defined as an output of the Physical layer. It is comprised of a 10-bit wide data bus, two receive byte clocks, an optional enable comma detection and a comma detect indication. The receive clocks operate at 53,125 MHz and are 180° out of phase with each other. The 106,25 MBaud receive data is presented to the Transmission protocol layer relative to the rising edge of each of the two receive byte clocks.

Two other signals complete the definition of the 10-bit interfaces: The first is the wrap or loopback signal, this is defined as an input to the Physical layer and causes the serialized transmit data to be looped back to the auxiliary receiver inputs. The second is the lock to reference signal, this signal is defined as an input to the Physical layer and forces the receiver PLL to lock to the reference clock.

### 4.1 Data flow

The 10-bit data presented to the Physical layer shall be serially transmitted sequentially to the cable plant bit 0 through bit 9, the relationship of transmit bits and the 8B/10B characters are described in annex N of FC-PH.

The receiver in the Physical layer shall receive and frame data at an arbitrary byte boundary until a comma sequence is received. The receiver shall realign its current byte boundary, if necessary to that of the received comma. This process is referred to in this document as "byte alignment". During the byte alignment process the Physical layer may delete up to 4 characters in order to align the correct receive clock and the data byte containing the comma character (byte 0). This process is referred to as "byte slipping".

## 4.2 Electrical interface signals

The Interface signals listed below shall comprise the minimum set of signals which must be supplied for compliance with this Technical Report.

### 4.2.1 TX[0,9]

TX[0,9] is the 10-bit parallel transmit data presented to the Physical layer for serialization and transmission onto the media. The order of transmission is TX[0] first, followed by TX[1] through TX[9].

### 4.2.2 TBC

TBC is the 106,25 MHz transmit byte clock. This byte clock is used to latch data into the Physical layer for transmission. If this clock is used as the transmitter PLL reference, it shall have the same  $\pm 100$  ppm tolerance as the REFCLK. TBC shall be frequency locked to REFCLK.

### 4.2.3 EWRAP

EWRAP shall causes the Physical layer devices to electrically loop serialized transmit data to the deserializer. The primary serial outputs on the transmitter shall be held in a static state during EWRAP operation. EWRAP may be tied low (function disabled) by the Transmission protocol layer.

### 4.2.4 RX[0,9]

RX[0,9] is the 10-bit parallel receive data presented to the Transmission protocol layer for further processing. The receive data byte 0 containing the comma character shall be byte aligned to RBC[1]; this is to say that byte 0 is in phase with RBC[1].

### 4.2.5 RBC[0]

RBC[0] is the 53,125 MHz receive byte clock that the protocol device shall use to latch the bytes 1 and 3 of the receive data word. This clock may be stretched during byte and word alignment, and shall not be truncated or slivered.

### 4.2.6 RBC[1]

RBC[1] is the 53,125 MHz receive byte clock that the protocol device shall use to latch the bytes 0 and 2 of the receive data word. RBC[1] is 180° out of phase with RBC[0]. This clock may be stretched during byte and word alignment, and shall not be truncated or slivered.

#### 4.2.7 COM\_DET

COM\_DET signal is an indication that the data byte (byte 0 of word 0) associated with the current RBC[1] contains a valid comma character. The Physical layer shall be required as a minimum, to detect the 7-bit comma+ character. The Physical layer shall provide this signal as an output, but the Transmission protocol layer may optionally ignore use of the signal as an input.

#### 4.2.8 -LCK\_REF

-LCK\_REF causes the Physical layer receiver to lock its PLL to REFCLK. The Physical layer shall be frequency locked within 500  $\mu$ s. This function may optionally not be utilized in the Physical layer (i.e., auto-lock to reference), but the 500  $\mu$ s frequency lock requirement is still valid.

#### 4.2.9 REFCLK

REFCLK is the 106,25 MHz transmit PLL reference

clock. The frequency tolerance for this clock shall be  $\pm 100$  ppm. REFCLK is used by the transmitter PLL to generate the 1 062,5 MHz bit rate clock. REFCLK is used by the receiver when -LCK\_REF is active. REFCLK may be the same signal as TBC.

#### 4.2.10 EN\_CDET

EN\_CDET enables the Physical layer to perform the byte alignment function on the comma sequence. When EN\_CDET is asserted the byte alignment function is operational. The Physical layer may have the byte alignment function always enabled.

### 4.3 Signal definitions

The signals listed below in table 1 shall be required at the specification interface, but all signal functions may not be utilized by the Physical or Transmission protocol layers.

**Table 1 - Signal definitions**

Symbol	Signal Name	Signal Type:	Active Level
TX[0:9]	Transmit Data	Input	H
TBC	Transmit Byte Clock	Input	↑
EWRAP	Enable Wrap	Input	H
RX[0:9]	Receive Data	Output	H
RBC[0]	Receive Clock	Output	↑
RBC[1]	Receive Clock	Output	↑
COM_DET	Comma Detect	Output	H
-LCK_REF	Lock to Reference	Input	L
REFCLK	Reference Clock	Input	↑
EN_CDET	Enable Comma Detect	Input	H

## 4.4 Reserved control signals

Table 2 list the 10-bit interface control signals and allowed combinations.

**Table 2 - Reserved control signal combinations**

EWRAP	-LCK_REF	EN_CDET	Interpretation
L	L	L	Undefined
L	L	H	Lock receiver PLL to REFCLK
L	H	L	Normal operation; COM_DET disabled
L	H	H	Normal operation; COM_DET enabled
H	L	L	Undefined
H	L	H	Undefined
H	H	L	Loop transmit data to receiver; COM_DET disabled
H	H	H	Loop transmit data to receiver; COM_DET enabled

## 5 Electrical definitions

### 5.1 TTL/CMOS characteristics

Table 3 documents the required DC parametric attributes required of all TTL/CMOS inputs to the Physical layer and the DC parametric attributes associated with the TTL/CMOS outputs of the Physical layer.

The inputs levels to the Physical layer may be greater than the power supply level [(i.e., 5V output driving  $V_{OH}$  into a 3.3V input), tolerance to mismatched input levels is optional. Physical layer devices not tolerant of mismatched inputs levels that meet table 3 requirements are still regarded as compliant.

**Table 3 - TTL/CMOS electrical characteristics**

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu A$	$V_{CC} = \text{Min}$	2,4	3,0	$V_{CC}$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 1\text{mA}$	$V_{CC} = \text{Min}$	GND	0,25	0,6	V
$V_{IH}$	Input High Voltage			2,0	-	$V_{CC}^1 + 10\%$	V
$V_{IL}$	Input Low Voltage			GND	-	0,8	V
$I_{IH}$	Input High Current	$V_{CC} = \text{Max}$	$V_{IN} = 2,4\text{V}$	-	-	40	$\mu A$
$I_{IL}$	Input Low Current	$V_{CC} = \text{Max}$	$V_{IN} = 0,4\text{V}$	-	-	600	$\mu A$
$C_{IN}$	Input Capacitance			-	-	4,0	pf
$t_R$	Clock Rise Time	0,8V to 2,0V		0,7	-	2,4	ns
$t_F$	Clock Fall Time	2,0V to 0,8V		0,7	-	2,4	ns
$t_R$	Data Rise Time	0,8V to 2,0V		0,7	-	-	ns
$t_F$	Data Fall Time	2,0V to 0,8V		0,7	-	-	ns

<sup>1</sup> Refers to the driving device power supply.

### 5.2 Valid signal levels

All AC measurements are made from the reference voltage level (1,4V) of the clock to the valid input or output data levels.

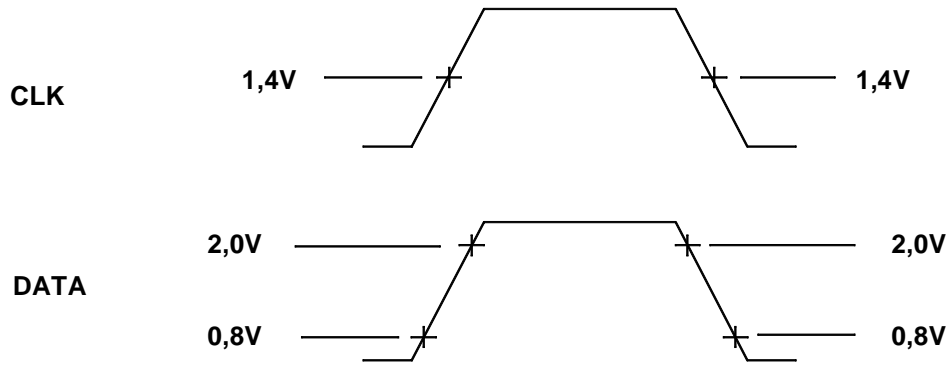


Figure 2 - Input output valid level for AC measurements

### 5.3 Rise and fall time definition

The rise and fall time definition for TBC, RBC and Data are shown below in figure 3.

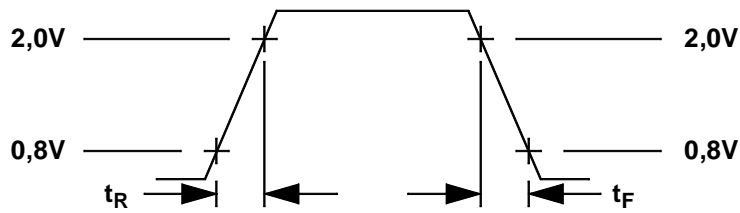


Figure 3 - Rise and fall time definition

### 5.4 TTL/CMOS load

All AC measurements are assumed to have the output load of 10 pF.

## 6 Transmit interface

### 6.1 Transmit data (TX[0,9])

The ten TX signals [0,9], carry data from the protocol device to the Physical layer transmit device to be transmitted on to the media. Refer to annex H of FC-PH for the proper transmission order. All 10-bit data presented to the Physical layer shall conform to the 8B/10B code as specified in tables 22 and 23 of FC-PH.

### 6.2 Transmit interface timing

The transmit interface timing in table 4 defines the Physical layer input. All transitions in figure 4 are specified from the Transmit Byte Clock midpoint to valid input signal levels.

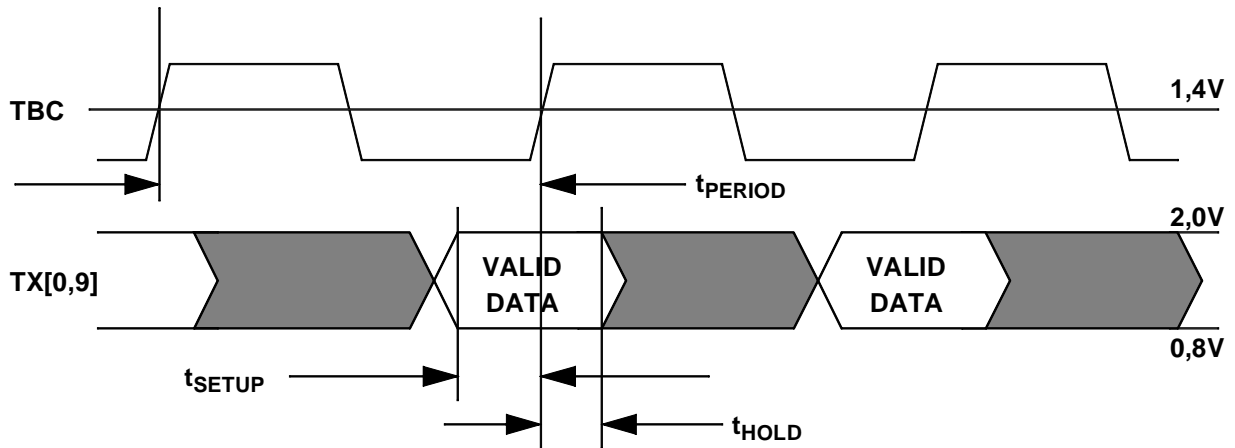


Figure 4 - Transmit interface timing diagrams

Table 4 - Transmit interface timing

Parameter	Description	Min	Typ	Max	Units
$t_{PERIOD}$	TBC Period <sup>1</sup>	-	$\frac{1}{106,25}$	-	MHz
$t_{SETUP}$	Data Setup to $\uparrow$ TBC	2,0	-	-	ns
$t_{HOLD}$	Data Hold from $\uparrow$ TBC	1,5	-	-	ns
$t_{DUTY}$	TBC Duty Cycle	40		60	%
1 $\pm$ 100 ppm tolerance on TBC.					

## 7 Receive interface

The receive interface timing in table 6 defines the Physical layer output. All transitions in figure 5 are specified from the Receive Byte Clock reference level (1.4V) to valid output signal levels.

### 7.1 Receive data (RX[0,9])

The ten RX signals [0,9] carry parallel data from the receiver in the Physical layer to the protocol device for further processing. Byte 0 of the receive data shall be valid during the positive edge of the receive clock (i.e. RBC[1] is HIGH). This provides a method for word alignment for protocol devices not utilizing the comma detect output from the receiver for that function. All data transferred across this interface shall conform to 8B/10B code as specified in tables 22 and 23 of FC-PH.

### 7.2 COM\_DET

The COM\_DET signal indicates that the receiver in the Physical layer has detected a comma sequence and that the byte (byte 0 of word 0) associated with the current positive edge of the clock (RBC[1]) contain a comma character. In order to provide this functionality, the Physical layer receiver may delete one or more characters if RBC[1] is out-of-phase with the received comma sequence. This allows RBC to be stretched an additional 1-byte (i.e, byte slip) so that on the next received comma sequence RBC[1] will be in-phase.

The receiver in the Physical layer shall be required to detect as a minimum, 7-bit comma+ (0011111). As a maximum, the two comma sequences or positive and negative disparity K28.5 detection is also allowed.

The K28.5 comma, as defined in FC-PH clause 11.4, has both a positive and negative disparity codings, i.e., comma+ and comma-, as shown in table 5.

### 7.3 Receive byte clock (RBC[0], RBC[1])

The receive byte clocks are supplied to the protocol device from the receiver in the Physical layer, and shall be derived from the recovered bit clock. RBC[0] shall be 180° out of phase with RBC[1]. During byte re-alignment the receive byte clocks may be stretched to the new byte boundary and shall not be slivered or truncated.

**Table 5 - Comma sequence definition**

Comma	Comma character									
	R X 0	R X 1	R X 2	R X 3	R X 4	R X 5	R X 6	R X 7	R X 8	R X 9
Comma+	0	0	1	1	1	1	1	x	x	x
Comma-	1	1	0	0	0	0	0	x	x	x

Table 6 specifies a receive byte clock drift ( $t_{DRIFT}$ ) which shall apply under all input conditions to the receiver (including invalid or absent input signals). However, the restriction shall not apply when the receiver is re-aligning to a new byte boundary and the receive clocks are being stretched to a new byte boundary to avoid short pulses. During the re-alignment process the receive byte clocks slow a fixed amount, depending on the offset of the new comma sequence and then return to the nominal frequency.

### 7.4 Receive interface timing

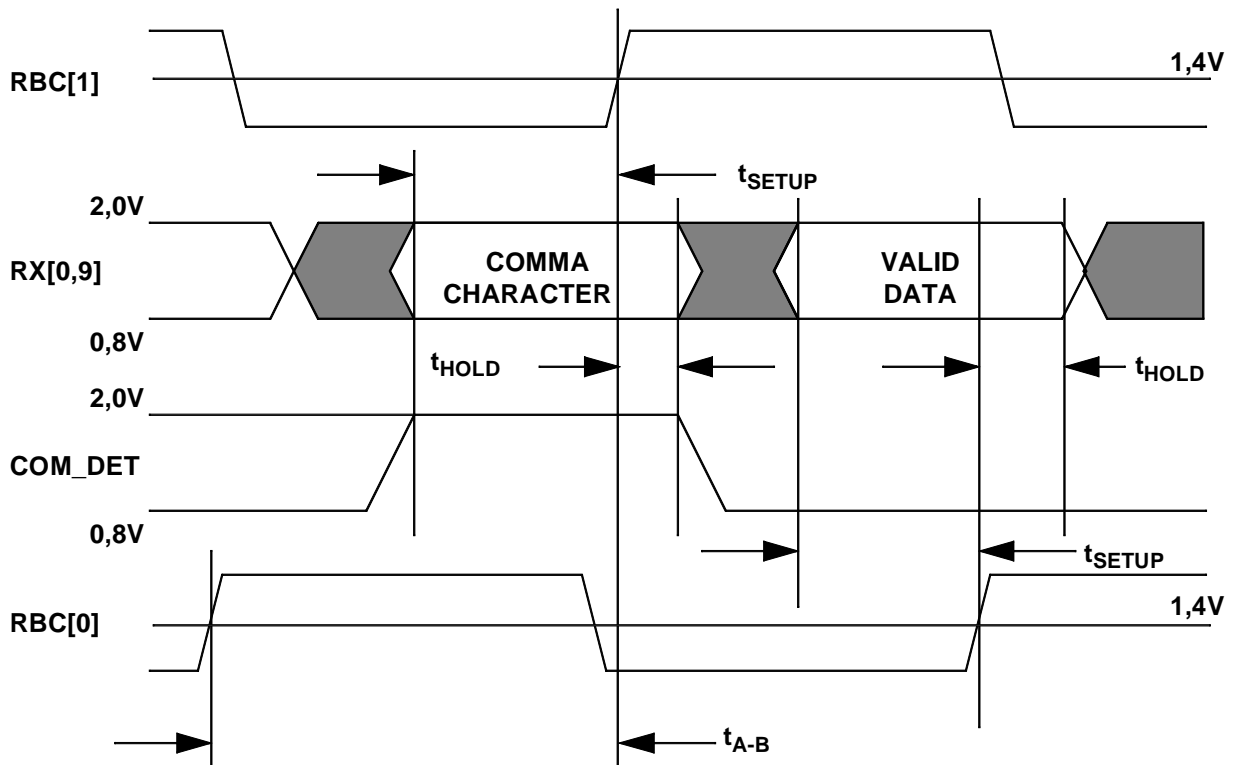


Figure 5 - Receive interface timing diagram

Table 6 - Receive interface timing

Parameter	Description	Min	Typ	Max	Units
$t_{FREQ}$	RBC Frequency	-	53,125	-	MHz
$t_{DRIFT}$	RBC Drift Rate <sup>1</sup>	0,2	-	-	us/MHz
$t_{SETUP}$	Data Setup Before $\uparrow$ RBC	3	-	-	ns
$t_{HOLD}$	Data Hold After $\uparrow$ RBC	1,5	-	-	ns
$t_{DUTY}$	RBC Duty Cycle	40	-	60	%
$t_{A-B}$	RBC Skew	8,9	-	9,9	ns

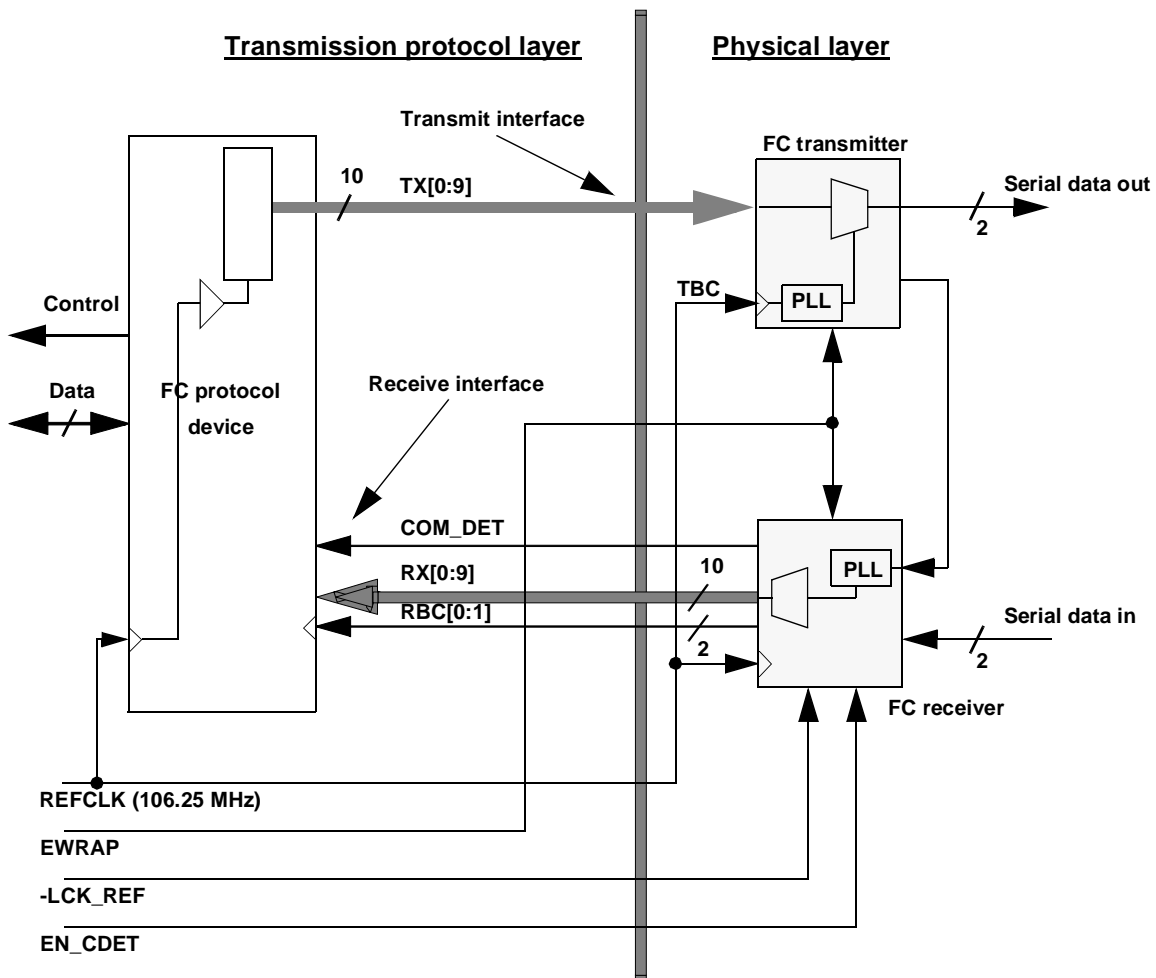
<sup>1</sup>  $t_{DRIFT}$  is the (minimum) time for RBC to drift from 54 MHz to 55 MHz or 52 MHz to 51 MHz from the RBC lock value. It shall apply under all input signal conditions (except where noted in 7.2), including invalid or absent input signals, provided that the receiver PLL was previously locked to REFCLK or to a valid input signal.

**Annex A**  
(informative)  
**Clocking methods**

This annex describes the allowable clocking methods for the 10-bit interface. The clocking is critical for proper interface operation and is thus illustrated here for clarity.

**A.1 TBC = REFCLK**

The clocking scheme shown in figure A.1 illustrates the case where the REFCLK is used as both PLL references, Transmission protocol layer master clock, and the Transmit Byte Clock (TBC). The Transmit Data (TX[0:9]) is assumed to be clocked out of the Transmission protocol layer using a distributed clock derived from the REFCLK input.



**Figure A.1 - Clocking scheme for TBC = REFCLK**

### A.2 TBC sourced by protocol device with separate REFCLK

The clocking scheme shown in figure A.2 illustrates the case where the REFCLK is used as both PLL references, and the Transmission protocol layer master clock. The Transmit Byte Clock (TBC) is a

derivative of REFCLK and sourced from the Transmission protocol layer to the Transmit Interface synchronous with the transmit data. TBC shall be frequency locked to REFCLK. The Transmit Data (TX[0:9]) is assumed to be clocked out of the Transmission protocol layer using a distributed clock derived from the REFCLK input.

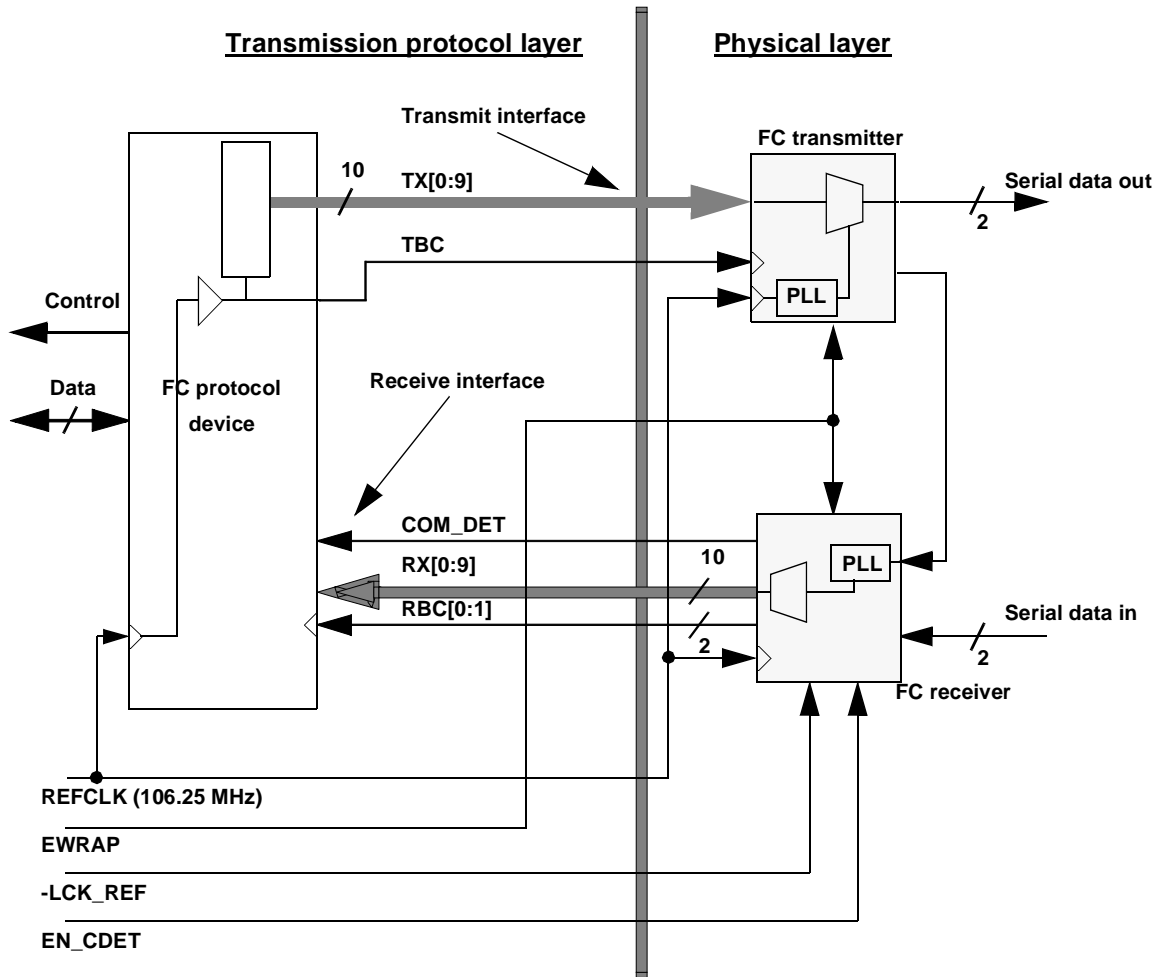


Figure A.2 - Clocking scheme for TBC sourced from Transmission protocol layer

### A.3 TBC sourced by protocol device

The clocking scheme shown in figure A.3 illustrates the case where the REFCLK is used as a PLL reference for the receiver only, and the Transmission protocol layer master clock. The Transmit Byte Clock (TBC) is a derivative of REFCLK and sourced from the Transmission protocol layer to the Transmit Interface synchronous with the transmit

data. TBC shall be frequency locked to REFCLK. The transmitter uses TBC as the transmit PLL reference, and thus must be suitable source for clock synthesis. The Transmit Data (TX[0:9]) is assumed to be clocked out of the Transmission protocol layer using a distributed clock derived from the REFCLK input.

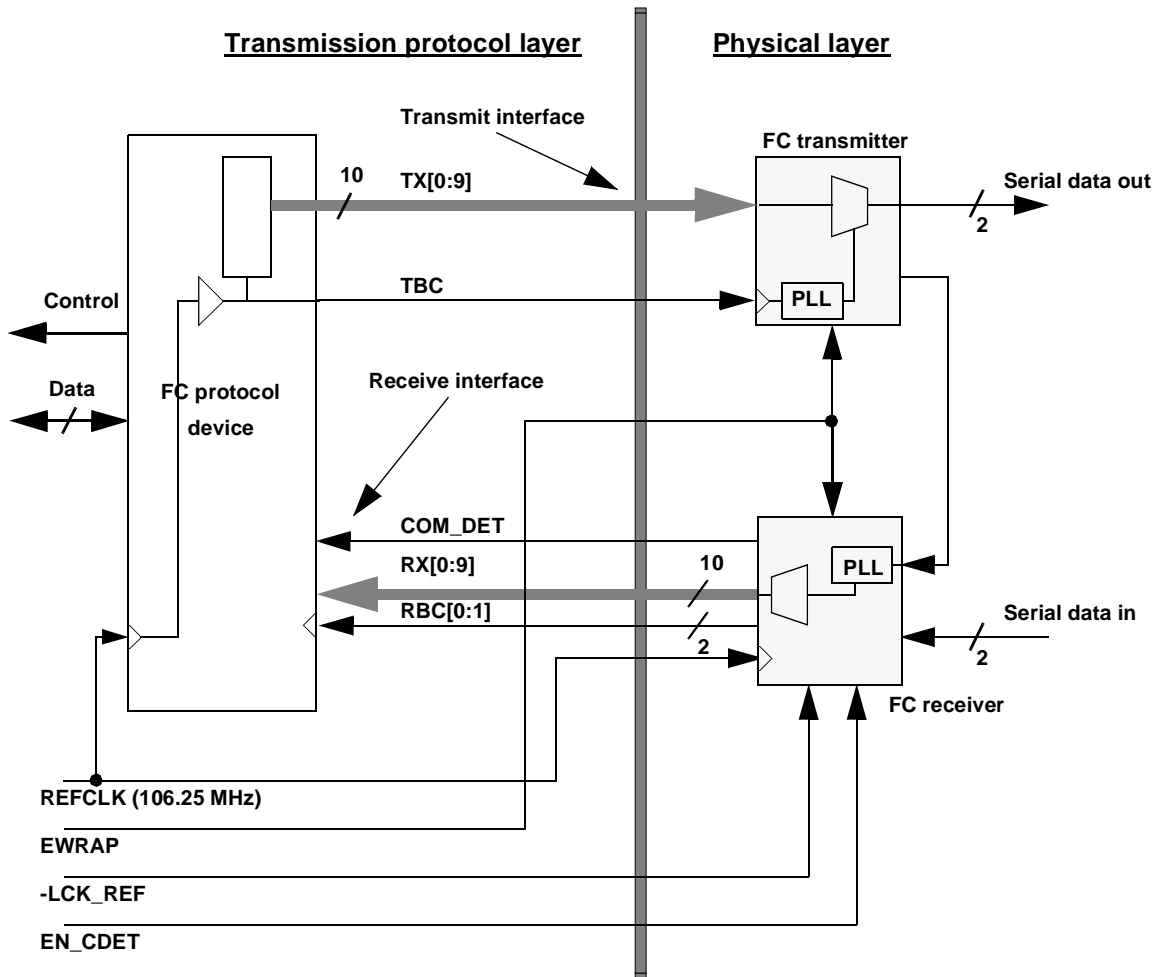


Figure A.3 - Clocking scheme for TBC clocking only